CLAIMS

What is claimed:

1. A method of fabricating a microelectronic die, comprising:

manufacturing transistors in and on a semiconductor substrate; and

stressing a channel of each transistor after the transistors are manufactured

2. The method of claim 1, wherein a tensile stress is applied to each channel.

3. The method of claim 1, wherein the channels are stressed by at least partially removing a portion of a handle substrate to which the semiconductor substrate is attached.

4. The method of claim 3, wherein an intermediate substrate is located between the semiconductor substrate and the handle substrate, the intermediate substrate having a lower CTE than the handle substrate.

5. The method of claim 4, wherein the intermediate substrate is made of diamond.

6. The method of claim 1, further comprising:

forming an intermediate substrate on a handle substrate;

allowing the intermediate substrate and handle substrate to cool, the

intermediate substrate having a different CTE than the handle substrate;

connecting the semiconductor substrate to the intermediate substrate; and

at least partially removing the handle substrate.

7. The method of claim 6, wherein the intermediate substrate and the handle substrate bow into a first shape when allowed to cool, and the semiconductor substrate and the intermediate substrate bow into a final shape when the handle substrate is removed.

8. The method of claim 7, further comprising:

changing the first shape into a second shape with less bow than the first shape before the semiconductor substrate is connected to the intermediate substrate.

9. The method of claim 8, wherein the first shape is changed into the second shape by applying a compensating layer.

10. The method of claim 9, wherein the compensating layer is made of silicon.

11. The method of claim 9, wherein the compensating layer is formed on major surfaces of both the intermediate substrate and the handle substrate but has a different CTE on the intermediate substrate than on the handle substrate.

12. The method of claim 1, further comprising:

singulating the semiconductor substrate after the channels are stressed.

13. A method of fabricating a microelectronic die, comprising:

forming a first combination wafer, including a handle substrate and an intermediate substrate on the handle substrate;

allowing the first combination wafer to cool, the intermediate substrate having a lower CTE than the handle substrate so that the combination wafer bows into a first shape;

forming a compensating layer on the combination wafer to form a second combination wafer, allowing the second combination wafer to cool, the compensating layer having a CTE which, compared to the CTEs of the handle substrate and the intermediate substrate, changes the first shape into a second shape with less bow;

connecting a semiconductor substrate to the second combination wafer; and

at least partially removing the handle substrate to change the second shape into a third shape and create a stress in the semiconductor substrate.

14. The method of claim 13, further comprising:

forming a plurality of transistors in and on the semiconductor substrate before removing the handle substrate.

15. The method of claim 13, wherein the intermediate substrate is made of diamond.

16. The method of claim 13, wherein the compensating layer is made of silicon.

17. The method of claim 13, wherein the compensating layer is formed on major surfaces of both the intermediate substrate and the handle substrate but has a different CTE on the intermediate substrate than on the handle substrate.

18. A combination wafer, comprising:

a handle substrate;

an intermediate substrate on the handle substrate; and

a semiconductor substrate on the intermediate substrate, wherein at least partial removal of the handle substrate changes a shape of the semiconductor substrate.

19. The combination wafer of claim 18, wherein a tensile stress is crated in the semiconductor substrate when the handle substrate is removed.

20. The combination wafer of claim 18, wherein the intermediate substrate has a CTE which is lower than a CTE of the handle substrate and a CTE of the semiconductor substrate.

21. The combination wafer of claim 20, wherein the intermediate substrate is made of diamond.